

(57) An amplifier device (9) for use with a photodetector (15) for amplifying wave energy signals received by the photodetector and converted into electrical signals includes a first amplifier (25) having its input connected to a junction between the photodetector and first (17) and second (19) photodetector load impedances. A feedback amplifier (29) connected to the output of the first amplifier provides a feedback voltage to the first load impedance when in its first mode of operation and effectively reduces the voltage feedback to the first load impedance when in its second mode of operation. A switching device (21) effectively switches the second load impedance in and out of circuit with the photodetector to change the effective photodetector load impedance and alter the bias voltage to the feedback amplifier. As a consequence, the feedback amplifier is able to operate in either of its first or second modes of operation, respectively switching the amplifier device from a good sensitivity, broad bandwidth transimpedance amplifier to a follower amplifier of improved dynamic range. Other forms of transducer may replace the photodetector.

FIG. 1.

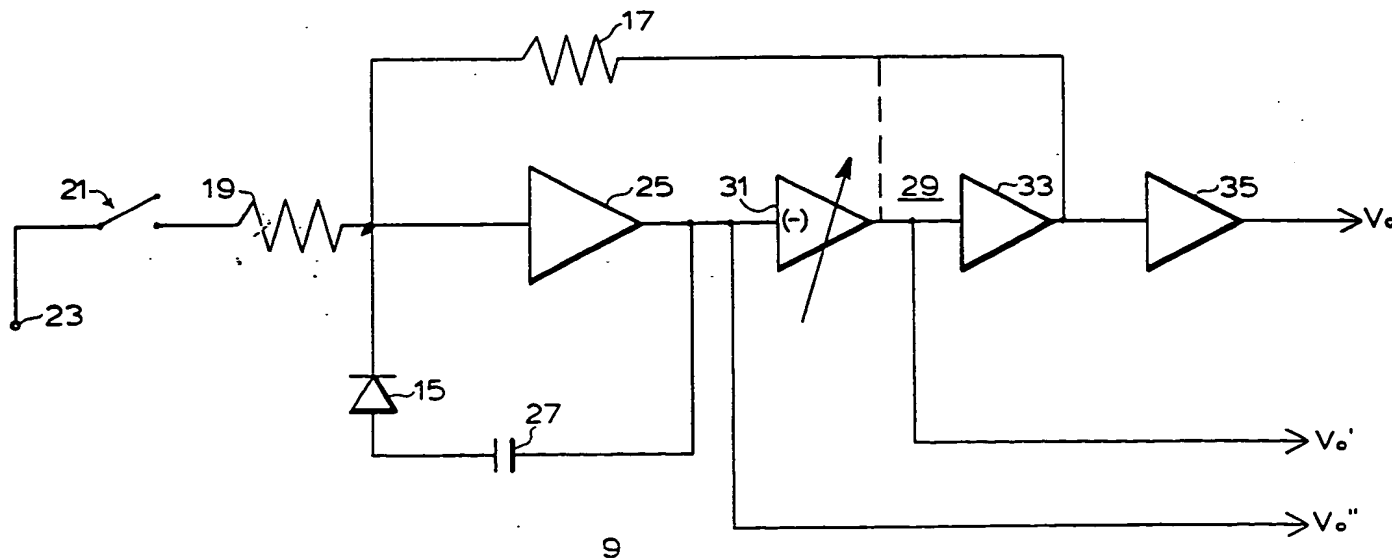
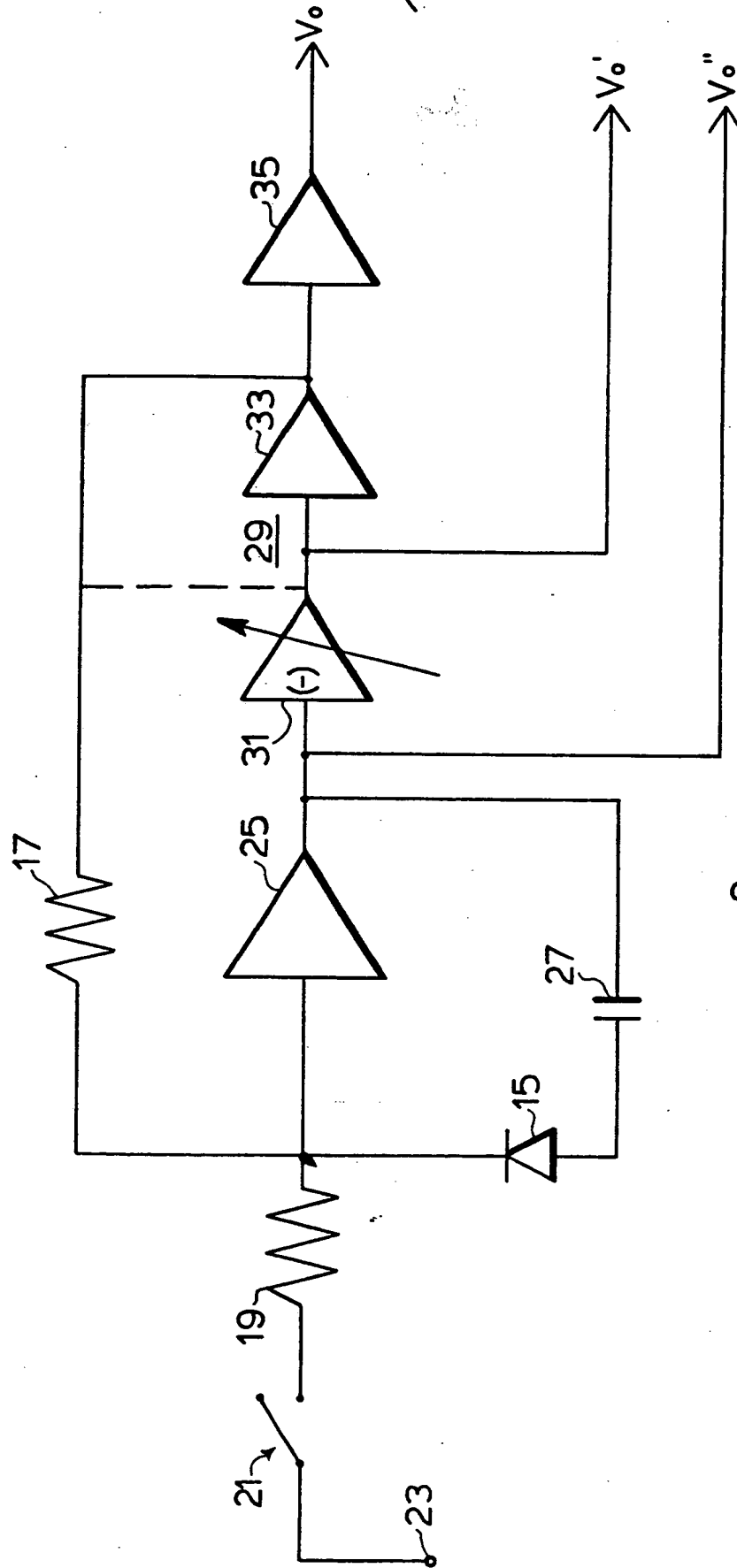


FIG.1.



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FIG.2.

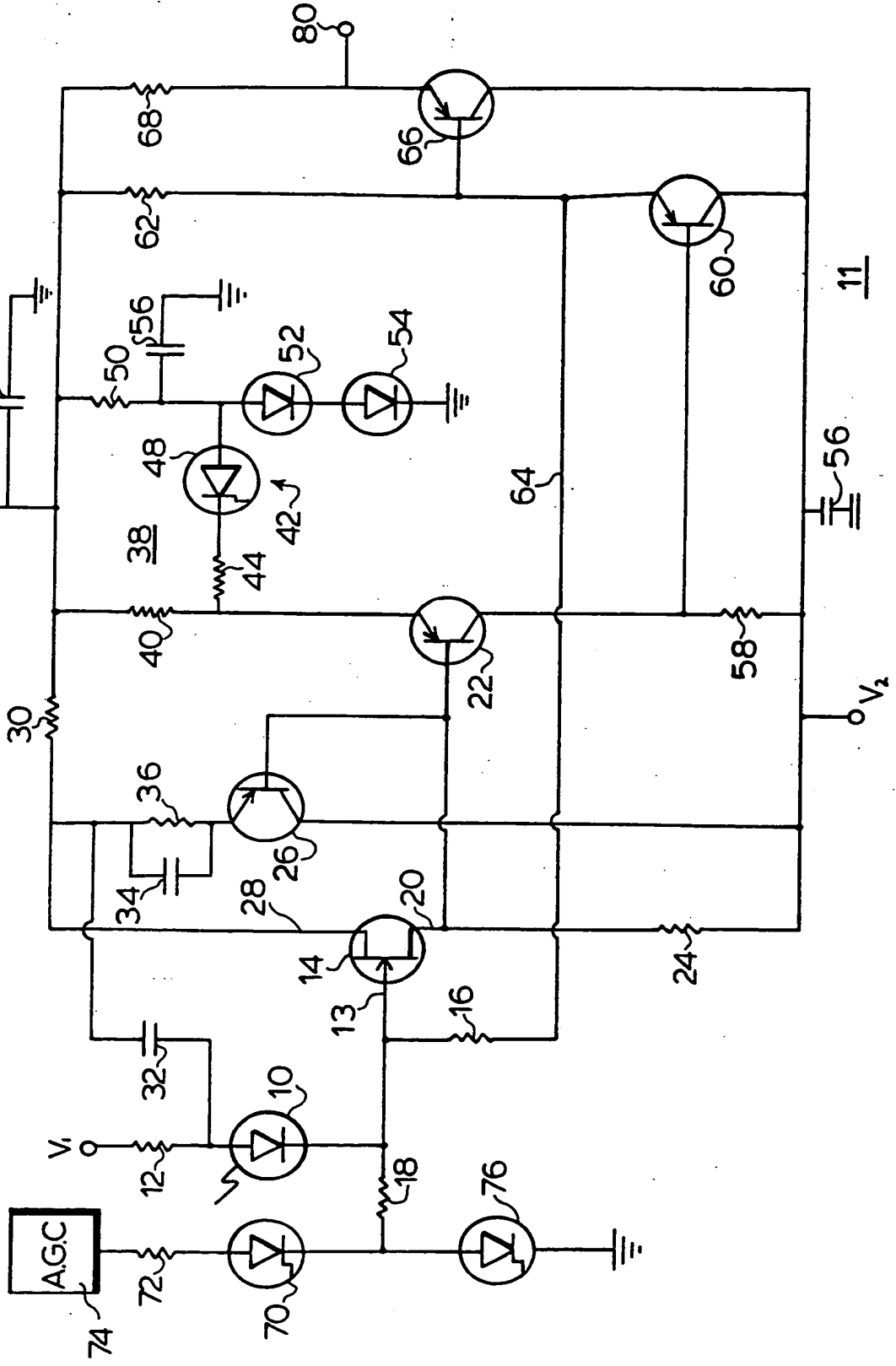
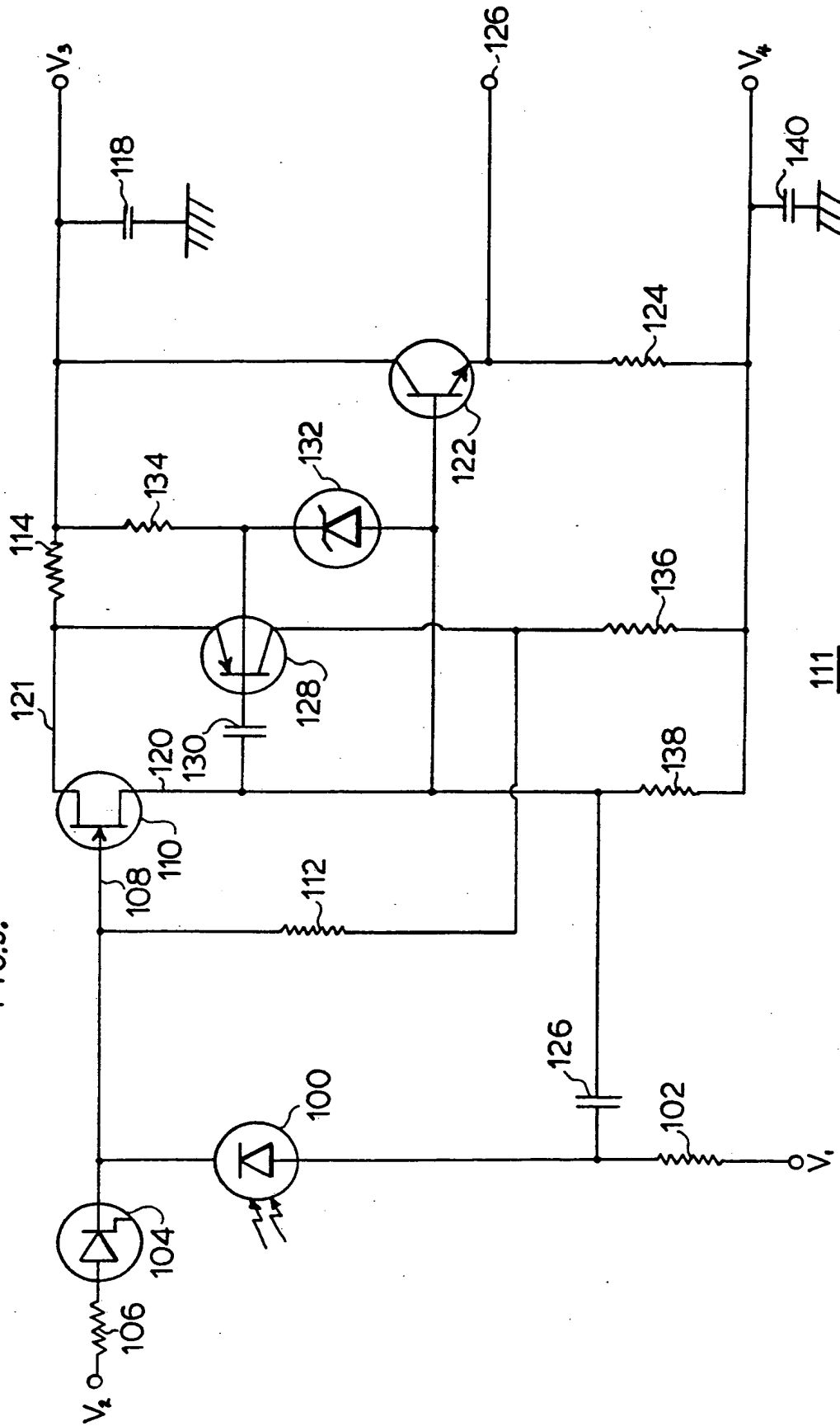


FIG. 3.



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SWITCHABLE MODE AMPLIFIER FOR WIDE DYNAMIC RANGE

The present invention relates to an amplifier for use in a receiver of an optical electric circuit. More specifically, the present invention
5 relates to an amplifier that is switchable between a broad bandwidth transimpedance mode and a follower mode of improved dynamic range.

Amplifiers and preamplifiers of signals detected by transducers, particularly photodiodes,
10 inherently include noise that effects the signal. Transducers such as germanium, silicon and InGaAs photodiodes have capacitance as their dominant impedance term. It is well known that the bandwidth of the amplifier is inversely proportional to the
15 input capacitance and the load resistance of the transducer. It is desirable, therefore, to reduce the effective input capacitance as well as the load resistance to improve the operating bandwidth of the amplifier. These reductions however, effect both the
20 noise performance and the response of the system.

A number of circuit arrangements have been devised to neutralize the effects brought about by input capacitances particularly in the low signal voltage input levels. One such circuit arrangement is
25 disclosed in U. S. Patent 3,927,383 issued December 16, 1975 to Fjarlie et al. In the circuit

arrangements disclosed, the photodiode is connected across the gate and source of a field effect transistor (FET). The source electrode of the FET is connected to the input of a negative feedback amplifier which feedbacks voltage through a load resistor connected to the gate of the FET. By connecting the photodetector across the gate and source electrodes of the FET a positive feedback is provided which neutralizes the input capacitance inherent in the photodetector by minimizing the voltage or potential variations across the photodetector due to the input wave energies applied to the photodetector. Further, the negative feedback reduces the effective impedance of the load resistor.

Another circuit arrangement is disclosed in U.S. Patent 4,535,233 issued August 13, 1985 to Abraham. The circuit disclosed therein is similar to that in U.S. Patent 3,927,383 except that an additional buffer amplifier is provided after the feedback amplifier. While these transimpedance amplifiers have provided an amplifier having good sensitivity and broad bandwidth operation, these amplifiers have a limited dynamic range.

There is described herein an amplifier suitable for use with a photodetector, such as in a fibre optic receiver. The amplifier is switchable between a transimpedance mode and a follower amplifier mode. The dynamic range of the amplifier can be improved by switching from a low power transimpedance mode to a high power follower mode.

In accordance with one aspect of the present invention there is provided an amplifier, switchable

between a broad bandwidth transimpedance mode and an improved dynamic range follower mode, for amplifying wave energy signals received and converted to electrical signals by a transducer. The amplifier

5 includes first amplifier means having an input coupled to a junction between the transducer and a first transducer load impedance means. The amplifier further includes second amplifier means coupled to the output of the first amplifier means and having its

10 output coupled to the first load impedance means. The second amplifier means is operable in a first mode to provide voltage feedback to the input of the first amplifier through the first impedance means. The amplifier includes output means coupled to the output

15 of the first amplifier means to provide an output signal in response to the receipt of the wave energy signals sensed by the transducer. The amplifier further includes a second transducer load impedance means connected to the junction between the transducer, the

20 first load impedance means and the input of the first load amplifier means. The second load impedance has a value which is less than that of the first load impedance. The second amplifier means is operable in a second mode to effectively reduce the voltage feedback

25 to the input of the first amplifier means. Switch means is connected to the second load impedance means to switch the second load impedance means in and out of circuit with the

transducer to effectively change the load impedance of the transducer and to respectively operate the second amplifier means in its first and second modes which respectively switches the amplifier between its
5 transimpedance and follower modes of operation.

In accordance with another aspect of the present invention there is provided an amplifier, switchable between a broad bandwidth transimpedance mode and an improved dynamic range follower mode, for
10 amplifying wave energy signals. The amplifier includes a field effect semiconductor device having a gate, drain, and source electrode. The device operates in a stable state at a gain approaching unity. The amplifier further includes a transducer
15 for generating an electrical current in response to receipt of the wave energy, one end thereof being coupled to the gate electrode and the other end thereof being coupled to a transducer biasing potential. The amplifier includes a negative feedback
20 amplifier coupled to the source electrode of the device. The feedback amplifier is operable in a first mode to generate a negative feedback voltage in response to the electrical current of the transducer. A first transducer load impedance is coupled between
25 the gate electrode of the device and the negative feedback amplifier and output buffer means is coupled to the source electrode of the device for providing an output signal in response to the receipt of the wave energy by the transducer. A second transducer load impedance is

coupled at one end to the gate electrode of the device. The second load impedance is connected at its other end to a biasing potential and the second transducer load impedance is less than the first
5 transducer load impedance. The negative feedback amplifier is operable in a second mode to effectively reduce the negative feedback voltage to the first transducer load impedance. Switching means is associated with the
10 second load impedance to effectively switch the second load impedance in and out of circuit with the gate electrode of the device to change the load impedance of the transducer, and the bias of the negative feedback amplifier to respectively operate the
15 negative feedback amplifier in its first and second modes which switches the amplifier respectively between its transimpedance and follower modes.

It should be understood that the term "coupled", as used throughout the specification and
20 claims, means that two components may be either directly connected to each other or indirectly connected through one or more intermediate components.

It should be understood that the term "follower mode" as used throughout the specification
25 and claims, means a follower amplifier that may invert or not invert the signal.

Advantage is found by switching the second transducer load impedance in and out of circuit. When the second transducer load impedance is switched into the circuit, this causes a reduction in the effective load resistance seen by the transducer which allows the amplifier to detect higher power signals and increase the dynamic range of the amplifier. The switching of the lower second load impedance in parallel with the higher first load impedance also changes the D.C. bias voltage applied through the first amplifier means to the second amplifier means. As a result in a change in the bias voltage applied to the second amplifier means the gain of the second amplifier means is substantially reduced or the second amplifier means may be switched off in its second mode of operation. As a result, the amplifier changes from a transimpedance amplifier having good sensitivity over broad bandwidth operation to a follower amplifier of improved dynamic range. Thus, while the amplifier in its transimpedance mode tends to operate well at amplifying low power signals detected by the transducer this amplifier will not saturate when high power signals are received since the amplifier can be switched into its follower mode where the sensitivity of the amplifier is reduced and the power level required to saturate the amplifier is increased due to the change in the transducer load impedance. Thus, the amplifier because of its follower mode of operation is said to have an improved dynamic range.

For a better understanding of the present invention reference may be had by way of example to the accompanying diagrammatic drawings in which:

Figure 1 is a schematic diagram of a wide

dynamic range amplifier embodying the present invention;

Figure 2 is a circuit diagram of the preferred embodiment of the amplifier; and

5 Figure 3 is a circuit diagram of an alternate embodiment of the amplifier;

Figure 1 illustrates a schematic diagram of a switchable mode amplifier 9.

10 The amplifier 9 includes a transducer in the form of a photodetector 15 for receiving energy signals and converting them to electrical signals. Connected to the output of the photodetector 15 is a first load impedance in the form of a feedback
15 resistor 17 and a second load impedance in the form of a resistor 19 which can be switched in and out of circuit by switch means 21 connected to a suitable biasing potential at 23.

 The signal received and converted by
20 transducer 15 is first passed through first amplifier means 25. The signal is positively coupled back through coupling capacitor 27 to the other side of the photodiode 15 so as to neutralize the input capacitance inherent in the photodetector 15 and
25 thereby increase the bandwidth operation of the amplifier. The first amplifier means 25 is preferably a unity gain amplifier.

 The signal is then fed from the first amplifier means 25 through a second amplifier means 29
30 which includes a variable gain inverting amplifier 31 and optionally a unity gain buffer amplifier 33. The signal can be fed back to the input of the first amplifier means 25 via resistor 17 from either amplifier 31 or optionally amplifier 33. Lastly, if
35 desired the signal can pass through a further unity gain buffer amplifier 35. Thus the output signal can

be taken optionally at outputs V_o , V_o' or V_o'' depending on the operation of the circuit.

At low power signal reception, amplifier 9 operates as a transimpedance amplifier when switch means 21 is open as shown in Figure 1. In this mode of operation the signal is fed back via feedback resistor 17 and the load impedance seen by the photodetector 15 is effectively that of the feedback resistor 17 divided by the combined gain of amplifier 25, 31 and 33..

At high power signal reception, amplifier 9 operates as a follower amplifier once resistor 19 is switched into the circuit by switch means 21 closing. Once resistor 19 is switched into the circuit the effective load impedance seen by photodetector 15 is resistor 19 in parallel with resistor 17.

The value of resistor 19 is chosen to be less than that of resistor 17 and is preferably considerably less than that of resistor 17; at least two orders of magnitude. As a result, the load resistance seen by photodetector 15 is reduced decreasing the output signal by 40 dB and thereby increasing the dynamic power range over which the amplifier may operate. It should be understood that the values of load resistors 17 and 19 can be chosen so that the amplifier 9 operates at desired gain/bandwidth requirements. Also, the DC bias potential applied through the first amplifier means 25 to the variable gain amplifier 31 changes when resistor 19 is switched into circuit. By changing the bias voltage applied to the variable gain amplifier 31, the gain of amplifier 31 may be reduced, effectively reducing feedback through resistor 17, or the amplifier 31 may be turned off. In the event amplifier 31 is turned off, the output signal is taken at V_o'' . In the event gain is reduced from anywhere in

the order of 10 to 50 to about 0.5, the output may be taken at V_o' or V_o . With this order of reduction in the gain, the dynamic range of the amplifier may be increased by as much as 40 dB.

5 Referring to Figure 2 there is shown a preferred circuit for the wide dynamic range amplifier for receiving and amplifying wave energy signals. The amplifier shown generally at 11 includes a photodetector or diode 10 having its anode terminal
10 connected to a bias voltage V_1 through a biasing resistor 12. The cathode of the photodiode 10 is connected to the gate electrode 13 of a first amplifying means preferably comprising a field effect transistor (FET) 14. Also connected to the gate
15 electrode 13 of FET 14 is a first load impedance or resistor 16 and a second load impedance or resistor 18. The source electrode 20 is connected to voltage potential V_2 via a biasing resistor 24. The source electrode 20 of FET 14 is further connected to
20 the input of the second amplifier means comprising the base of a bipolar feedback transistor 22. The drain electrode 28 of FET 20 is connected to voltage potential V_3 through a suitable biasing resistor 30. Positive feedback is provided to the
25 drain electrode 28 from source 20, amplifier 26 and filtering capacitor 34. The source electrode 20 of the FET 14 is also positively coupled to the anode of photodiode 10 through transistor 26, filtering capacitor 34 and biasing resistor 36, and filtering
30 capacitor 32. This positive bootstrapping of the photodiode capacitance, gate to drain and gate to source capacitance of FET 14 to the anode of photodiode 10 effectively neutralizes the capacitance of the photodiode 10 and that developed across the
35 gate to source of FET. Both FET 14 and the transistor amplifier 26 have gains approaching unity.

A second, feedback, amplifying means is provided by the circuitry associated with transistor 22. The transistor 22 has its gain controlled by a variable impedance circuit shown generally at 38. This impedance circuit 38 includes a parallel connection between a first resistor 40 and branch impedance 42. Branch impedance 42 includes a resistor 44 connected to the cathode of shottky diode 48. The anode of shottky diode 48 is connected through resistance 50 to the voltage supply V_3 and is connected to two commonly oriented series connected diodes 52 and 54. Diode 52 has its anode connected to the anode of the shottky diode 48 and diode 54 has its cathode connected to ground. The capacitors shown generally at 56 throughout the circuit provide filtration and stability for the amplifier. The operation of circuit 38 will be described in more detail when the operation of the amplifier of Figure 2 is described.

The collector of transistor 22 has a bias resistance 58 connected to the voltage supply V_2 . The output of the signal is taken from the collector and enters through the base of transistor or unity gain buffer amplifier 60. The emitter of buffer amplifier 60 is suitably biased by resistance 62. A feedback path is provided to resistor 16 from the emitter of buffer amplifier 60 and the feedback path is shown generally by numeral 64. The emitter of amplifier or transistor 60 is connected to a further unity gain buffer amplifier 66. The buffer amplifier 66 has a bias resistor 68 associated therewith. The output 80 of the amplifier 11 is connected to the emitter of transistor 66.

Looking to the extreme left hand side of the circuit of Figure 2 there is shown two schottky diodes 70, 76 connected at their junction to second

load resistance 18. These diodes constitute the sensitivity switching means in this embodiment of the invention. The first schottky diode 70 has its anode connected through suitable biasing resistance 72 to a variable or automatic gain control (AGC) circuit 74. The cathode of diode 70 is connected to the anode of schottky diode 76 and the second load resistance 18. The cathode of schottky diode 76 is connected to ground potential.

10 It should be understood that standard component parts can be used for the circuitry shown in Figures 1, 2 and 3 and that the values of the components can be chosen so as to meet required gain and bandwidth requirements of the amplifier.

15 During the operation of the amplifier shown in Figure 2, light wave energy impinging on the photodiode 10 is converted into electrical current. This signal is fed through the FET 14 which has approximately unity gain. The signal is then fed from the source 20 of the FET through the feedback amplifier system comprising transistors 22 and 60. Transistor 60 acts as a buffer buffering the feedback circuit from transistor 22. The signal is fed back through to the input or gate electrode of FET 14 along path 64 and resistance 16. The signal is also fed through transistor 66 to the output shown generally at 80. Transistor 66 basically acts as a buffer isolating the output from the remainder of the circuit. In this mode of operation when the signal is fed back through resistor 16, the amplifier 11 of Figure 2 is operating as a transimpedance amplifier and the diodes 70 and 76 are operating as a switch which effectively maintains the resistance of the second load resistor 18 out of the circuit. The amplifier typically has a gain in the range of 20 to 35 decibels. The load resistance is determined by

the effective resistance seen across resistor 16. Since FET 14 and amplifier 60 are unity gain amplifiers, the overall gain of the amplifier is determined for the most part by the gain associated with transistor 22. When the switch comprising diodes 70 and 76 has a low input at the voltage input 74, the diodes 70 and 76 are non-conducting making resistor 18 appear as an open circuit having an infinite load. This causes the bias voltage associated with transistor or feedback transistor 22 to be at a value that diode 48 of variable impedance circuit 38 is conducting. As a result, the gain associated with the transistor 22 will approximately equal the effective collector resistance divided by the effective emitter resistance. The emitter resistance will be resistor 40 in parallel with resistor 44 and the effective resistance of diode 48. Preferably, resistors 40 and 58 will be chosen to be in the same order of magnitude. Resistor 44 and the effective resistance of diode 48 may be considerably lower than that of resistor 40. Further, resistor 44 may not be needed. For example when resistor 40 is about 2200 ohms, resistor 44 is about 22 ohms, the diode 48 resistance is about 25 ohms and the resistor 58 is about 1000 ohms the gain of transistor 22 will be about 22 when diode 48 conducts and about .45 when diode 48 does not conduct. It should be understood that the values of the components may be chosen such that the gain of transistor 22 is preferably in the range of 10 to 50 when diode 48 is conducting and is preferably about .45 when diode 48 is not conducting.

When the power of the signal received from the light impinging upon diode 10 increases to a value above a predetermined value sensed by the AGC circuit 74, the amplifier 11 is switched from its

transimpedance mode to its follower mode of operation. The AGC applies a higher bias voltage to the diodes 70 and 76 causing conduction of the diodes. As a result the second impedance

5 resistance 18 is connected to a virtual ground due to the conduction of diode 76. The second impedance 18 is now in circuit with the first load impedance 16. The second load impedance is preferably about 1 kilohm whereas the effective first load impedance is

10 about 100 kilohms. A parallel combination of this circuit resistance will provide for an effective resistance for the photodiode 10 to be in the order 1 kilohm. The drop in effective photodetector load impedance acts to offset the rise in current generated

15 by the photodetector due to increased energy signals impinging the photodetector. As a result the voltage output of the amplifier remains within acceptable limits.

Once the second load resistance 18 is

20 connected in circuit, the DC bias voltage through the unity gain FET 14 to the base of transistor 22 increases. This causes the DC emitter voltage of transistor 22 to increase and causes diode 48 to become non-conducting removing resistor 44 from the

25 circuit. As a result the effective emitter resistance of transistor 22 is increased and the gain of transistor 22 decreases to preferably about .45. This represents an overall gain in the dynamic range of about 25 to 40 dB. With the gain reduction of

30 transistor 22, feedback through resistor 16 is reduced significantly. In effect the amplifier 11 operates as an inverting follower amplifier when transistor 22 operates in its second mode having reduced gain.

In summary, the circuit of Figure 2 provides

35 capacitive bootstrapping via transistor 26, so as to neutralize the capacitance associated with the

photodiode 10. Further, due to the switching of diodes 70 and 76, the effective load resistance or impedance of the photodiode 10 is switched, the effective biasing of the amplifier is switched, and
5 hence the sensitivity of the amplifier switched between transimpedance and follower modes switching its dynamic power range by about 40 dB.

Referring now to Figure 3 there is shown an alternate circuit for realizing the present
10 invention. The photodiode is shown generally at 100 and has its anode connected to a biasing voltage potential V_1 through a biasing resistor 102. The cathode of diode 100 is connected to the cathode of a switching diode or schottky diode 104. A second load
15 resistance 106 is provided suitably biased to a switching voltage potential V_2 . In this embodiment diode 104 provides mode switching.

The cathodes of diodes 100 and 104 are connected to the gate electrode 108 of unity gain FET
20 transistor 110. The gate 108 of transistor 110 is coupled to a first load resistance 112 and to the second load impedance through diode 104.

The drain of FET 110 is connected through a suitable biasing resistor 114 to a biasing
25 potential V_3 . The biasing potential V_3 is provided with proper filter capacitance 118.

The source electrode 120 of FET 110 is connected directly to a unity gain buffer
amplifier 122. The emitter of the buffer amplifier or
30 transistor 122 has a suitable biasing resistor 124 which connects to a voltage source V_4 . The output of the emitter of transistor 122 is taken at 126 and provides the output for the amplifier. The source 120 of FET 110 is coupled in a positive fashion through
35 filtering capacitance 126 to the anode of photodiode 100. Coupled to the source electrode 120

is the base of amplifier transistor 128. The base of the transistor 128 is connected to the source via a parallel connection of a filter capacitor 130 and a zener diode 132. Zener diode and the base of transistor 128 are suitably biased via a biasing resistor 134.

The collector and emitters of transistor 128 are suitably biased via respective resistors 136 and 114. The source 120 of FET 110 is biased to a voltage supply V_4 by resistance 138.

The operation of the amplifier shown in Figure 3 normally operates as a transimpedance amplifier when diode 104 is in an open circuit mode. As a result the diode 100 load resistance is determined by load resistor 112. The signal received by diode 100 is converted into an electrical signal which passes the gate to source junction of FET 110 and out through the base emitter junction of transistor 122 to output 126. During this time feedback is provided via the zener diode which is conducting in its reverse breakdown mode maintaining transistor 128 conducting to provide a feedback path through its collector and resistor 112.

The capacitance associated with the diode 100 and the gate to source capacitance of FET 110 is positively fed back through capacitor 126 to the anode of diode 100 so as to neutralize these capacitance values and increase the bandwidth operation for the amplifiers shown in Figure 2.

When the input signal detected by photodetector 100 increases to a point where the circuit cannot properly amplify this signal, then voltage is applied at V_2 to cause the schottky diode 104 to turn on. As a result, load resistance 106 is brought into circuit in parallel with load resistance 112. Since load resistance 106

is considerably less than that of load resistance 112, the effective load impedance will be approximately equal to that of impedance 106. Since resistor 112 preferably has resistance in the order of 100 kilohms
5 and resistor 106 has a resistance in the order of 1 kilohm the overall signal gain reduction will be about 20 dB. Once resistor 106 is switched in circuit by diode 106 the biasing DC potential at the gate electrode of FET 110 increases which increases the
10 biasing DC voltage provided to the anode of zener diode 132. This results in the zener diode entering a non-conducting mode and shutting off the transistor 130. This effectively prohibits the feedback of voltage across load resistance 112
15 converting the resistance 112 from a feedback resistance to a biasing resistance for diode 104. At this time the amplifier of Figure 3 operates in a follower mode with reduced sensitivity or improved dynamic range.

20 It can be seen from the operation of the circuits shown in Figures 1, 2 and 3 that the amplifier has been provided where the overall gain or sensitivity of the amplifier can be decreased by switching the amplifier from a transimpedance
25 amplifier into a follower inverting or non-inverting amplifier.

CLAIMS:

1. An amplifier switchable between a broad bandwidth transimpedance mode and an improved dynamic range follower mode, for amplifying wave energy signals received and converted to electrical signals by a transducer including:

first amplifier means having an input coupled to a junction between the transducer and a first transducer load impedance means;

second amplifier means coupled to the output of the first amplifier means and having its output coupled to the first load impedance means, said second amplifier means being operable in a first mode to provide voltage feedback to the input of the first amplifier through the first impedance means, and being operable in a second mode to effectively reduce the voltage feedback to the input of the first amplifier means;

output means coupled to the output of the first amplifier means to provide an output signal in response to the receipt of the wave energy signals by the transducer;

a second transducer load impedance means connected to the junction between the transducer, the first load impedance means and the input of the first load amplifier means, the second load impedance being less than the first load impedance; and

switch means connected to said second load impedance means to switch said second load impedance means in and out of circuit with said transducer to effectively change the load impedance of said transducer and to respectively operate the second amplifier means in its first and second modes which respectively switches the amplifier between its transimpedance and follower modes of operation.

2. An amplifier as in Claim 1, wherein the second amplifier means has a bias applied thereto which is altered when the second impedance is switched into circuit to effectively switch the second amplifier into its second mode of operation reducing the voltage feedback to the first amplifier means.

3. An amplifier as in Claim 1, wherein the output of the first amplifier means is positively coupled to the transducer.

4. An amplifier as in Claim 1, wherein the second amplifier means is turned off in its second mode of operation.

5. An amplifier as in Claim 1, wherein the second amplifier means has a gain which is controlled by the switch means to reduce the voltage feedback, and the output means is coupled to the output of the first amplifier means via the second amplifier means.

6. An amplifier as in Claim 2, wherein the second amplifier means has a variable impedance circuit associated therewith and responsive to the bias voltage applied to the second amplifier means to alter the impedance of the variable impedance circuit and consequently change the gain of the second amplifier means.

7. The amplifier of any preceding claim wherein the feedback amplifier is a negative feedback amplifier.

8. An amplifier switchable between a broad bandwidth transimpedance mode and an improved dynamic range follower mode, for amplifying wave energy signals, including:

5 a field effect semiconductor device having gate, drain, and source electrodes, said device in use operating in a stable state at a gain approaching unity;

10 a transducer for generating an electrical current in response to receipt of said wave energy, one end thereof being coupled to said gate electrode and the other end thereof being coupled to a transducer biasing potential;

15 a negative feedback amplifier coupled to the source electrode of said device, said feedback amplifier being operable in a first mode to generate a negative feedback voltage in response to the electrical current of said transducer, and in a second mode to effectively reduce the negative feedback voltage to the
20 first transducer load impedance;

 a first transducer load impedance coupled between the gate electrode of said device and the negative feedback amplifier;

25 output buffer means coupled to the source electrode of said device for providing an output signal in response to the receipt of said wave energy by said transducer;

30 a second transducer load impedance coupled at one end to the gate electrode of said device, said second load impedance being connected at its other end to a biasing potential, said second transducer load impedance being less than the first transducer load impedance; and

switching means associated with said second load impedance to effectively switch said second load impedance in and out of circuit with the gate electrode of said device to change the load impedance of the transducer, and bias of the negative feedback amplifier to respectively operate the negative feedback amplifier in its first and second modes which switches the amplifier respectively between its transimpedance and follower modes.

9. An amplifier as in Claim 8, wherein the second transducer load impedance is considerably less than the first transducer load impedance.

10. An amplifier as in Claim 8, wherein the negative feedback amplifier comprises a transistor having its base coupled to the source electrode of said device and its collector coupled to the first transducer load impedance, the transistor turning off in the second mode of operation precluding the negative feedback voltage.

11. An amplifier as in Claim 10, wherein the transistor has a zener diode connected between the base of the transistor and the drain electrode of the device, the zener diode being operable between a conducting and non-conducting mode in response to changes in the bias voltage to switch the negative feedback amplifier between its first and second modes.

12. An amplifier as in Claim 8, wherein the negative feedback amplifier has a variable impedance circuit associated therewith responsive to the change in bias voltage to control the mode of operation of the negative feedback amplifier.

13. An amplifier as in Claim 8, wherein the negative feedback amplifier comprises a transistor having its base coupled to the source electrode of said device and its collector coupled to the first
5 transducer load impedance and the output of the switchable mode amplifier.

14. An amplifier as in Claim 13, wherein the collector of the feedback transistor has a resistance
10 element coupled thereto, and the emitter of the feedback transistor has connected thereto an impedance circuit comprising a first resistance connected in parallel with an impedance branch between the emitter
15 of the feedback transistor and a voltage supply, the impedance branch including a first diode having its anode connected to a junction of a second resistance connected to the voltage supply and an anode of a first
20 diode of a series pair of diodes oriented in the same direction with the cathode of the second diode of the series pair connected to ground, said first diode being
operable between conducting and non-conducting modes responsive to the bias voltage applied to the feedback
25 transistor to change the effective impedance of the impedance branch and thereby change the mode of operation of the feedback amplifier.

15. An amplifier as in Claim 8, wherein the other end of the transducer is coupled to the source and drain electrode of the device.

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16. An amplifier as in Claim 15 having a second transistor in circuit between the other end of the transducer and the source electrode of the device, the second transistor having its base connected to the
35 source electrode and its emitter connected to the other end of the transducer.

17. An amplifier as in Claim 14, wherein a third resistance is connected in series with the first diode.

5 18. An amplifier substantially as hereinbefore described with reference to Figure 1, Figure 2 or Figure 3 of the accompanying drawings.